Analysis and Design Considerations of Zero-Voltage and Zero-Current-Switching (ZVZCS) Full-Bridge PWM Converters

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Abstract*- — In this paper, a detailed analysis of the zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converters is performed. The differences of the zero-voltage-switching (ZVS) operation between the conventional ZVS full-bridge PWM converters and the ZVZCS full-bridge PWM converters are analyzed in depth. Circuit parameters that affect the soft-switching conditions are examined and the critical parameters are identified. Based on the analysis, practical design considerations are presented. The analysis and design considerations are verified by experimental results from a 630V/4kW converter operating at 80kHz.

I. INTRODUCTION

Recently, numerous soft switching techniques for the switching power converters have been proposed. These techniques reduce the switching losses enabling high frequency operation and consequently reducing the overall system size. Among those, the zero voltage switching (ZVS) full-bridge PWM converter with phase shift control has been the most popular topology for many applications [6,7]. It utilizes circuit parasitics such as the switch junction capacitance and the transformer leakage inductance to achieve ZVS of the primary switches without requiring additional resonant components. However, it has several drawbacks such as narrow ZVS range, reduction of effective duty cycle, and severe voltage ringing in the secondary rectifier side. Moreover, it is not suitable for high power applications using IGBTs, since IGBTs have high turn off switching loss caused by the tail current.

In an effort to improve the ZVS full-bridge PWM converter, a number of zero-voltage and zero-current-switching (ZVZCS) full-bridge PWM converters have been proposed for the last several years [1-5]. The ZVS of the leading-leg switches is achieved by a similar manner as that of the conventional phase shifted ZVS full-bridge PWM converters, while the zero-current switching (ZCS) of the lagging-leg switches is achieved by resetting the primary current during the freewheeling period. In the previous works, the ZVS operation of the ZVZCS full-bridge PWM converter has been known to be same with that of the ZVS full-bridge PWM converter, and only a few studies on the detailed analysis of the soft switching mechanism are found in the literatures. Since the ZVS mechanism of the ZVZCS full-bridge PWM converters is different from that of the conventional ZVS full-bridge PWM converter, different design considerations are required.

This paper investigates how the ZVS operation of the ZVZCS full-bridge PWM converters is different from that of the conventional ZVS full-bridge PWM converter. The interesting feature of the ZVZCS full-bridge PWM converters - the circulating current for ZCS can be self-adjusted according to the load conditions – is also studied. Circuit parameters that affect the soft-switching conditions are examined and the critical parameters are identified. Based on the analysis, practical design considerations are presented. The analysis and the design considerations are verified by experimental results from the 630V/4kW converter operating at 80kHz.

II. ANALYSIS

2.1 Review of Steady State Operation

Fig.1 shows the basic circuit diagrams of the ZVZCS full-bridge PWM converters [1-5]. The auxiliary circuits for ZCS are different for each converter. The ZVS of the leading-leg switches is achieved by the energy stored in the leakage inductance of the transformer, while the ZCS of the lagging-leg switches is achieved by reducing the primary current by discharging the holding capacitor during the freewheeling period.

To analyze the steady state operation, it is assumed that all components and devices are ideal and the output filter inductor is large enough to be regarded as a constant current source during one operating half-cycle. The theoretical waveforms are shown in Fig.2. All of the converters operate in the same way except that the holding capacitors are charged in different ways, respectively. The operation principles are changed slightly at light load condition, since the circulating current is self-adjusted according to the load condition. Thus, it is assumed that the converter operates at full load condition in the explanation of the circuit operation.

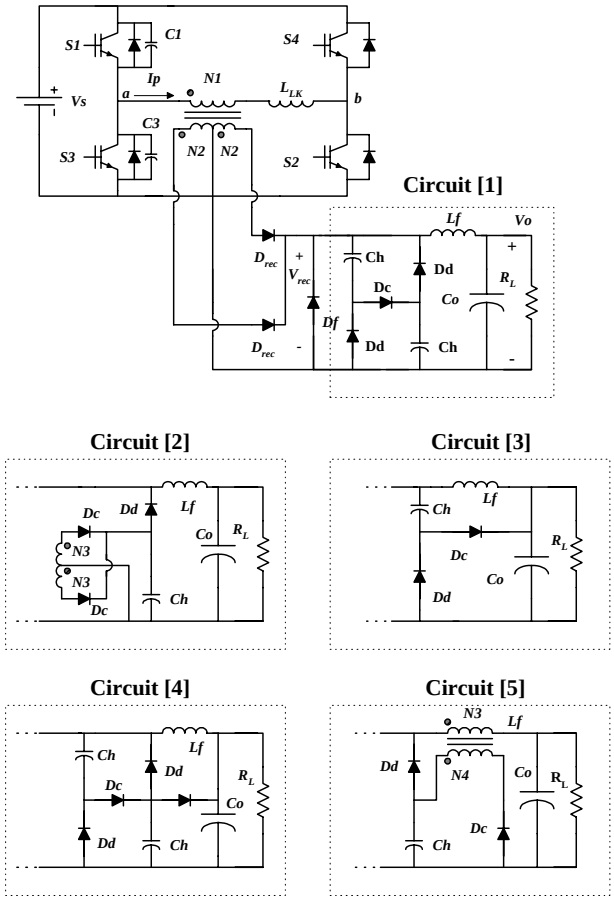


Fig. 1 Circuit diagram of ZVZCS FB PWM converter [1-5]

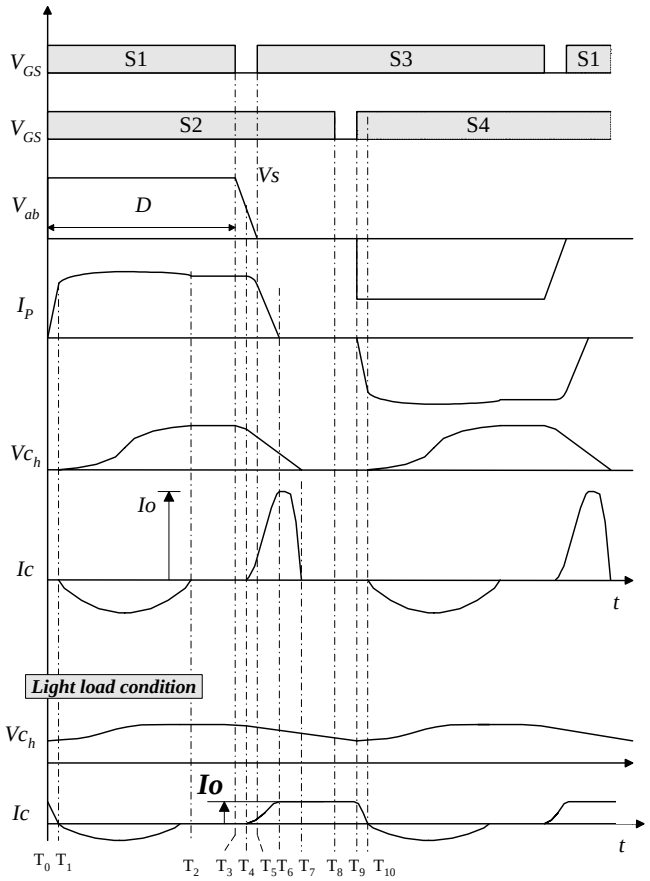


Fig. 2 Theoretical waveforms

Mode1 (T_0-T_1): S2 turns on and the input voltage, *Vs*, is applied to the leakage inductance of the primary side, L_{Lk}. The primary current I_P increases linearly until it reaches the reflected output inductor current.

Mode2 (T_1-T_2) : S1 and S2 are conducting and the power is transferred to the secondary. The holding capacitor C_h is charged through the auxiliary circuit by the resonance with the leakage inductance. At the end of this mode, holding capacitor is charged up to V_H, which is different for each converters and summarized in Table. I.

Mode3 (T_2-T_3) : When the current of Dc reduces to zero, Dc turns off with zero current and the holding capacitor voltage remains as charged in mode 2. The primary current is still transferred to the output.

Mode4 (T_3-T_4) : S1 turns off at T_3 and the primary current charges C1 and discharges C3. The voltage V_{ab} decreases linearly.

Mode5 (T_4-T_5) : When the rectifier voltage V_{rec} reaches V_H, the discharging diode D_d turns on and the rectifier voltage is clamped at the holding capacitor voltage. The transformer primary side voltage decreases at the same rate as before until it reaches zero, while the rectifier voltage, clamped at the holding capacitor voltage, decreases slowly. The difference between the primary side transformer voltage and the reflected secondary side voltage is applied to the leakage inductance L_{LK} and the primary current and voltage decrease.

Mode6 (T_5-T_6) : C_3 is completely discharged, and the switch S3 turns on with zero voltage. The entire reflected secondary voltage is applied to the leakage inductance and the primary current decreases more quickly. The primary current decreases until it reaches zero.

Mode7 (T_6-T_7) : When the primary current is completely reset, the rectifier diodes turn off and C_h supplies the whole load current. Thus, the rectifier voltage decreases quickly until it reaches zero.

Mode8 (T_7-T_9) : The holding capacitor is completely discharged and the output inductor current freewheels through the diode D_f. At T_8, S2 turns off with zero current.

TABLE I. The value of V_H for each converter

Converter [1]	$Vs\,(N_2/N_1)$
Converter [2]	$2Vs\,(N_2/N_1)$
Converter [3]	$2[Vs\,(N_2/N_1)-V_o]$
Converter [4]	$2[Vs\,(N_2/N_1)-V_o]$
Converter [5]	$2\,N_4/N_3\,(V_s\cdot N_2/N_1-V_O)$

2.2 Self-adjustment of the circulating current

It was assumed that the converter operates at full load condition in the explanation of the circuit operation. Under full load condition, the holding capacitor is completely discharged during mode 7 supplying the load current. In the full load condition, the charging current of the holding capacitor of mode 2 is obtained as follows ;

$$I_{Ch}(t) = -\frac{V_H}{2}\sqrt{\frac{C_h}{L_{lks}}}\sin(w_S t) \tag{1}$$

where $w_s = \frac{1}{\sqrt{L_{lks}C_h}}$ and L_{lks} is the leakage inductance of the secondary side.

However, as the load current decreases, the holding capacitor is not fully discharged during the mode 7 and the holding capacitor current continues supplying the load current until T_{10}. The difference between the maximum value (V_{ch}^{max}) and the minimum value (V_{ch}^{min}) of the holding capacitor voltage is obtained by integrating the discharging current of the holding capacitor as ;

$$\begin{aligned} &V_{Ch}^{\max} - V_{Ch}^{\min} \\ &= \frac{1}{C_h}\int_{T_4}^{T_{10}} I_{Ch}(t)dt \cong \frac{I_o}{C_h}(1-D)T_s/2 \end{aligned} \tag{2}$$

where Ts is the switching period and *Io* is the output current.

From (2), the charging current of the holding capacitor of (1) is changed at light load condition as follows:

$$\begin{aligned} I_{Ch}(t) &= -(V_{Ch}^{\max} - V_{Ch}^{\min})\sqrt{\frac{C_h}{L_{lks}}}\sin(w_s t) \\ &\cong -(1-D)\frac{T_s I_o}{2C_h}\sqrt{\frac{C_h}{L_{lks}}}\sin(w_s t) \end{aligned} \tag{3}$$

From (3), it can be seen that the circulating current charging and discharging the holding capacitor is decreased as the load current decreases, which means that the circulating current is self-adjusted according to the load condition.

III. DESIGN CONSIDERATIONS

3.1 ZVS conditions for the leading leg switches

In order to achieve ZVS of the leading leg switches, the transformer primary side voltage should decrease to zero during the dead time given by

$$T_{dead} > t_{m4} + t_{m5} \tag{4}$$

where $t_{m4} = T_4 - T_3 = nC_{eq}(\frac{V_S - nV_H}{I_o^{ZVS}})$ (5)

$$\begin{aligned} t_{m5} = T_5 - T_4 &= \frac{1}{w_b}\sin^{-1}(\frac{n^2 \cdot V_H C_{eq} w_b}{I_o}) \\ &= \frac{1}{w_b}\sin^{-1}(\frac{n^2 \cdot V_H}{I_o Z_c}) \end{aligned} \tag{6}$$

where $n = \frac{N_1}{N_2}$, $w_b = \frac{1}{\sqrt{L_{LK}C_{eq}}}$, $Z_c = \sqrt{\frac{L_{LK}}{C_h}}$, $C_{eq} = C_1 + C_3$, and C_1 and C_3 are the output capacitances of S1 and S3, respectively.

From (6), the minimum load current guaranteeing ZVS, I_o^{ZVS} is obtained as

$$I_o^{ZVS} = n^2 V_H\sqrt{\frac{C_{eq}}{L_{LK}}} \tag{7}$$

The ZVS ranges for different maximum holding capacitor voltages, V_H's are shown in Fig.3 as a function of C_{eq}. Basically, ZVS eliminates the capacitive turn-on loss and reduces the turn-off switching loss by slowing down the voltage rise and thereby reducing the overlap between the switch voltage and the switch current. While the turn-off switching loss of the leading leg switches can be reduced by adding an external snubber capacitor to the IGBTs, large C_{eq} limits the ZVS range as shown in Fig.3. Therefore, C_{eq} should be chosen by the trade-off between the ZVS range and the turn-off switching loss of the leading leg switches.

In case of the conventional full-bridge ZVS PWM converters, ZVS of the leading leg switches can be achieved even at light loads, because the anti-parallel diodes of the leading leg switches can always be turned on by the reflected current of the output filter inductor. The minimum load current guaranteeing ZVS of the leading leg switches is given by

$$I_o^{ZVS} = n^2 Vs\sqrt{\frac{C_{eq}}{L_f}} \tag{8}$$

where *Vs* is the input voltage and *Lf* is the output filter inductor. Since the energy stored in the output filter inductor is large enough to discharge the external capacitors of the leading leg switches, large external capacitors can be used ensuring ZVS at light loads. However, ZVS range of ZVZCS full-bridge PWM converters is relatively narrow, since the energy stored in the leakage inductor is used to discharge the external capacitors of the leading leg switches.

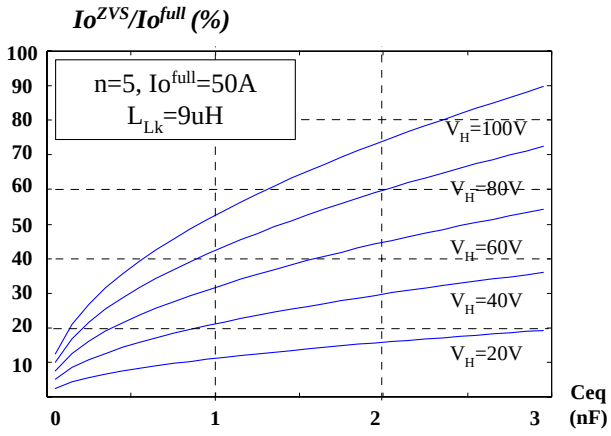


Fig.3 ZVS range for different V_H values

3.2 ZCS conditions for the lagging leg switches

Fig.4 shows the reset of the primary current for different holding capacitor values. In order to achieve zero current turn-off of the lagging leg switches, the energy of the holding capacitor should be large enough to reset the current through L_{LK}, and the primary current should be reduced to zero prior to the turn-off of the lagging leg switches. This relationship is obtained as

$$\frac{1}{w_b}\sin^{-1}\left[\frac{I_O \cdot Z_c}{V_H \cdot n^2}\cos(w_b t_{m5})\right] < \frac{T_S}{2}(1-D) \qquad (9)$$

As can be seen in (9) and Fig. 4, in order to guarantee ZCS, it is required to increase C_h or V_H. However, the maximum value of V_H is limited below input voltage reflected to the secondary, Vs/n, and too large C_h increases the circulating current that is indirectly transferred to the load through C_h. The effect of soft switching on the converter power loss is a trade-off between the reduced switching losses and the additional conduction loss caused by the soft switching. To achieve desirable efficiency improvement, it is required to minimize the additional conduction loss by designing Ch as small as possible.

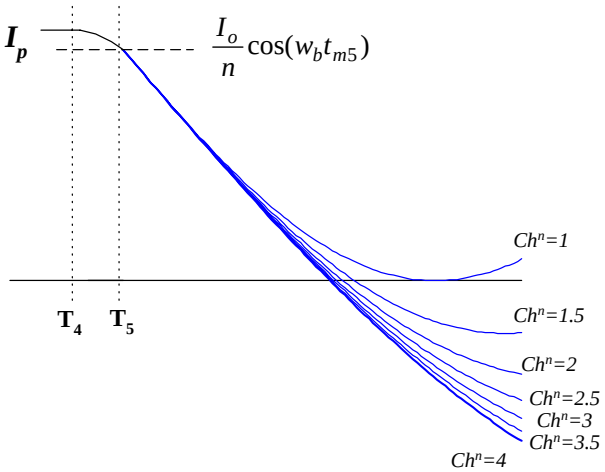
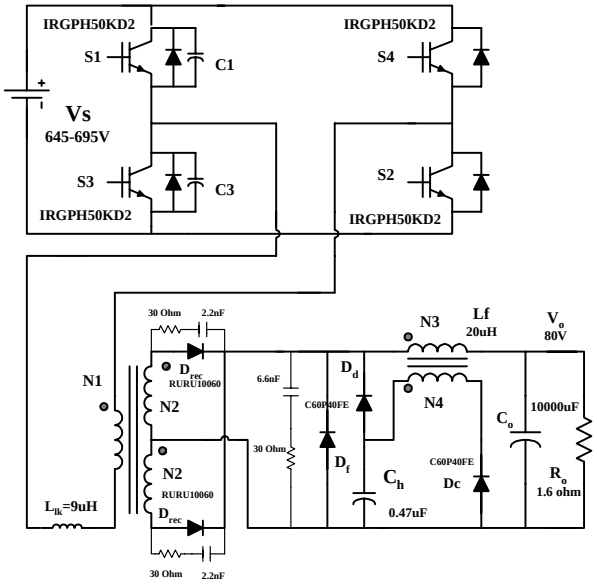


Fig.4 Reset of the primary current for different Ch values

IV. EXPERIMENTAL RESULTS

Among the various ZVZCS full-bridge PWM converters, the converter of [5] was taken as an example and built. The specifications and the designed component values are summarized in Fig.5. In order to reduce the turn off switching loss of the leading leg switches guaranteeing the maximum efficiency at full load, C_1 and C_2 are designed to be 0.47nF, and the ZVS is guaranteed down to 40% of the full load. If smaller external capacitors are used, the ZVS range can be widened. However, too small external capacitor results in high turn off switching loss.



Transformer	PE22EC90-Z , N1:N2=16:3, L_{LK}=9μH
Lf	PE22EC90-Z, 20μH, N3:N4=9:8,

Fig.5 schematic of the converter of [5]

Fig.6 compares efficiencies when the external capacitor is 0.47nF and when 0.1nF. When C_1 and C_3 are 0.1nF, the ZVS range is guaranteed down to 20% of the full load, which results in higher efficiency at light load. However, the efficiency is lower at full load, since the external capacitors do not slow down the leading leg switch voltage sufficiently. Fig.7 and Fig. 8 show the waveforms of the leading leg switches at full load and 30% load, respectively. As designed, ZVS is guaranteed at full load, while ZVS is lost below 40% load. Fig. 9 shows the zero current turn-off waveforms of the lagging-leg switch S2. The current through S2 is reduced to zero before the gating signal is disabled, and the switch S2 turns off with zero current.

Fig.10 and Fig.11 show the voltage and the current of the holding capacitor at full load and 25% load, respectively. At the full load condition, the holding capacitor is fully discharged during the freewheeling period, while not completely discharged at light load condition making the circulating current adaptively changed according to the load conditions.

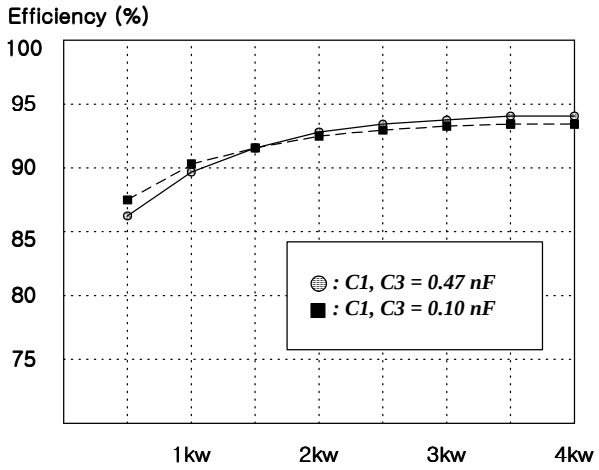


Fig. 6 Efficiency

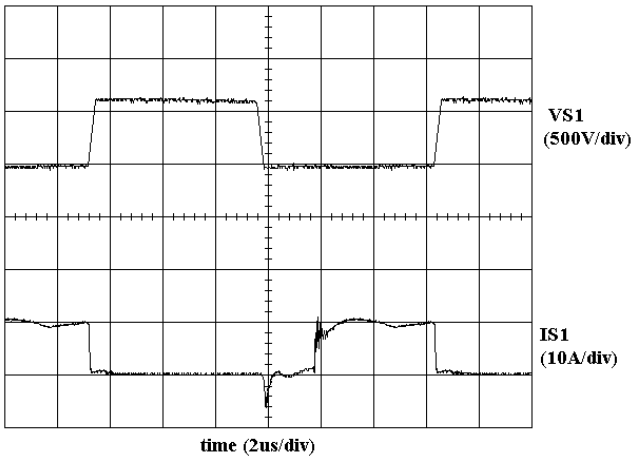


Fig. 7 Voltage and current waveforms of S1 (@full load)

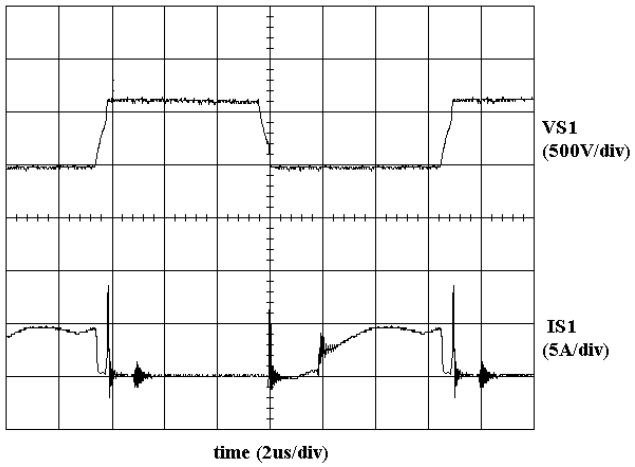


Fig. 8 Voltage and current waveforms of S1 (@30% load)

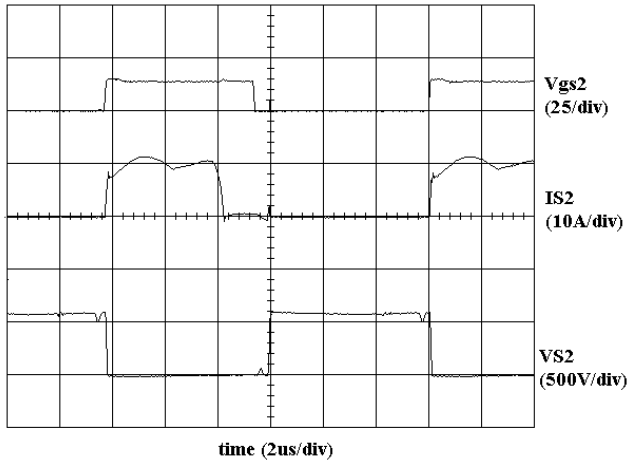


Fig. 9 Voltage and current waveforms of S2

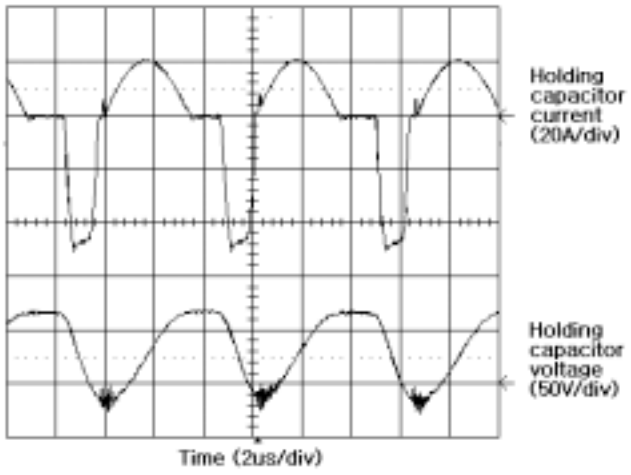


Fig.10 Current & voltage waveforms of Ch at full load

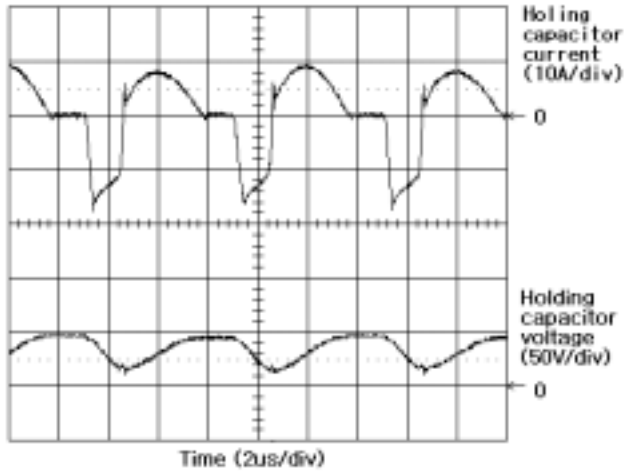


Fig.11 Current & voltage waveforms of Ch at light load

V. CONCLUSION

In this paper, the zero-voltage and zero-current-switching (ZVZCS) Full-bridge PWM converter was analyzed in depth. The difference of the zero-voltage-switching (ZVS) principle between the conventional ZVS full-bridge PWM converters and the ZVZCS full-bridge PWM converters was analyzed in detail. Circuit parameters affecting the soft-switching conditions were examined and the critical parameters were identified. Based on the analysis, practical design considerations were presented. The design procedures can be applied to the various kinds of ZVZCS full-bridge PWM converters [1-5]. The analysis and design considerations were verified by experimental results from a 630V/4kW converter operating at 80kHz.

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