# High-Efficiency Forward Transformer Reset Scheme Utilizes Integrated DC-DC Switcher IC Function

Author: Tiziano Pastore – Power Integrations GmbH – Germany

**Abstract:** This paper discusses a simple high-efficiency reset scheme for DC-DC forward converters, which is made possible by an integrated function of the *DPA-Switch* device. The capacitor reset scheme, in conjunction with the integrated Maximum Duty Cycle ($DC_{MAX}$) reduction function, provides a very simple, yet robust and highly efficient technique of resetting transformer-magnetizing flux. This technique will also be compared with the other commonly used reset methods.

Introduction:

*DPA-Switch*™, the industry's first monolithic DC-DC switcher IC with an integrated 200 V power MOSFET, eliminates 20 to 50 external components from high efficiency DC-DC converter designs, saving space and enabling higher power densities, while reducing design cost. It dramatically simplifies and eases the design process, enabling shorter design cycles while producing a more reliable solution.

Targeting 24 V / 48 V Distributed Power Architectures, the four-device family provides a wide input range (16 V to 75 V) and up to 100 W of output power. The innovative design of *DPA-Switch* integrates lossless current sensing, removing the need for current-sense resistors or expensive current-sense transformers. The devices can be configured in either Forward or Flyback topologies. Simplified synchronous rectification is possible, in the Forward topology, enabling efficiencies of up to 91%.

Transparent or built-in features of the IC include auto-restart for output overload and open loop protection, soft-start for minimum stress and overshoot at turn-on, cycle-skipping, down to zero load (no pre-load required), and auto-recovering hysteretic thermal shutdown. Three user-configurable pins allow the 7-leaded device to provide UV/OV sensing (meets ETSI standards), externally set accurate, primary current limiting, remote ON/OFF, synchronization to a lower external frequency, and internal frequency selection (300 or 400 kHz).

Low Output Voltage, dc/dc power conversion is dominated by one topology, the Forward Converter (see figure 1). Design engineers favour its relative simplicity and cost effectiveness. However, the non-ideal behaviour of the transformer is commonly seen as the main difficulty with the Forward converter. An ideal transformer has infinite inductance, which would prevent any magnetic flux build up in the core. However, the finite inductance of the real world transformer develops a positive magnetic flux accumulation, during the switch conduction period.

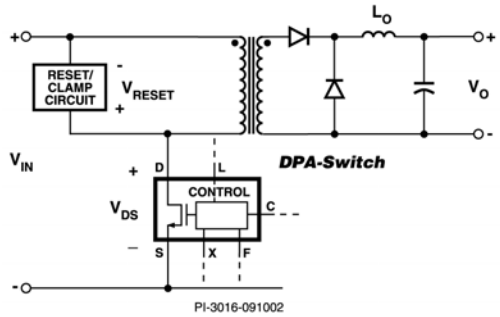


**Figure 1 –** Forward converter using *DPA-Switch*

To prevent core saturation, the flux must be reset by the end of each switching cycle (see figure 2). If this magnetising flux is not reset to zero each switching cycle, it will build up over consecutive cycles until the transformer core saturates. The maximum duty cycle reduction function of the *DPA-Switch* was designed so that maximum switch on-time is reduced sufficiently, as $V_{IN}$ increases, to ensure sufficient core reset time.

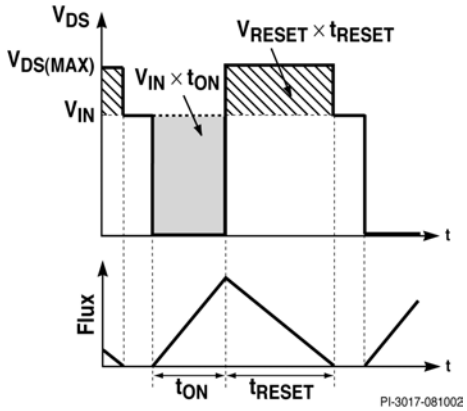


**Figure 2 -** Flux balance: $V_{IN}$ x $t_{ON}$ = $V_{RESET}$ x $t_{RESET}$

A commonly used reset technique is the so-called “1:1 reset winding” (see figure 3). An additional winding on the transformer allows the inductance demagnetizing energy to recirculate back into the primary side bulk capacitance, resetting the core.

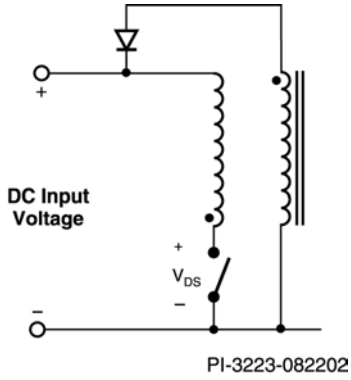


**Figure 3 –** Reset-winding schematic

This solution forces the maximum duty cycle to be no greater than 50% ($t_{ON}$ = $t_{RESET}$, see figure 4), since reset always takes the same amount of time as the initial flux buildup. Limiting low-line duty cycle increases RMS and peak currents in the primary, therefore an expensive MOSFET with very low $R_{DSon}$ is required and overall efficiency is affected. For an input voltage of 75 VDC a MOSFET with more than a 200 V breakdown threshold may be required (see figure 5), depending on the size of the leakage inductance spike.

This plus the added complexity, cost and size of an additional winding, makes this technique fairly impractical for low-cost, wide DC input voltage range designs.

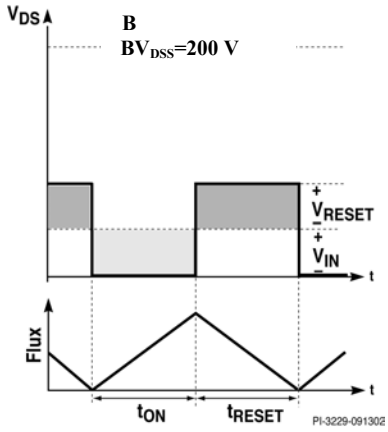


**Figure 4 –** Reset winding technique: at low line, it is limited to 50% maximum duty cycle

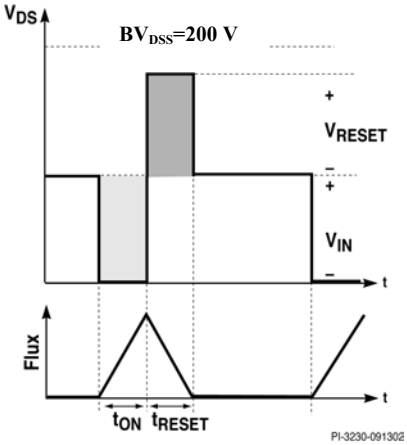


**Figure 5 -** Reset winding technique: at high line, high peak drain voltages result

A second reset method is an R-C-D clamp circuit (see figure 6).

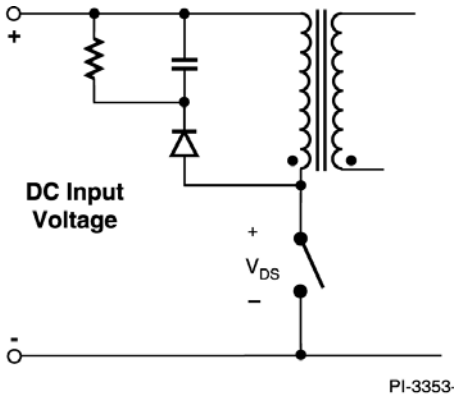


**Figure 6 -** R-C-D reset technique.

With this technique, the reset time and drain voltage are dependent on line and load conditions. In the worst-case, at maximum input voltage, a fast low-to-high load transition would suddenly cause switch on-time to increase and off-time (core reset) to decrease (ref figure 8). This would increase the voltage the MOSFET Drain would see and may prevent complete reset, allowing the core to creep into saturation, during the ensuing switching cycles. At low line, limited available reset voltage constrains the duty cycle to a lower percentage (see figure 7) than it could occupy, which increases RMS and peak MOSFET currents. Additionally, this scheme dissipates the demagnetizing energy, which limits overall converter efficiency.

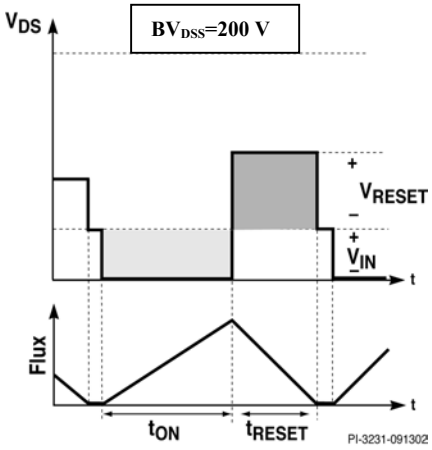


**Figure 7 -** R-C-D scheme at low line.

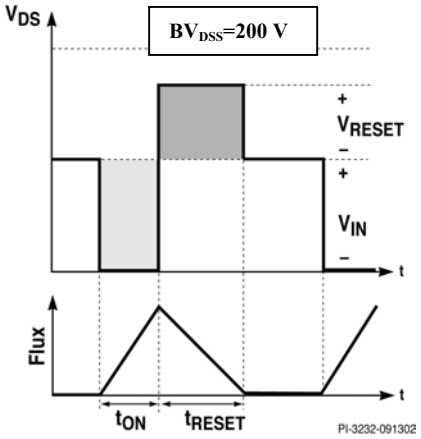


**Figure 8 -** R-C-D scheme at high line.

A third solution, which utilizes the $DC_{MAX}$ reduction function integrated onto the *DPA-Switch*, allows the recovery of the demagnetizing inductance energy, increasing the efficiency of the converter (see figure 9).

Capacitor $C_S$ (1 to 10 nF) is the main reset component. It stores the demagnetizing energy, until the core is reset, and then transfers the energy back into the core, as negative flux. $R_S$ damps oscillations. $C_S$ may not be required in synchronous rectification designs, due to gate capacitance performing the same “recycling” function.

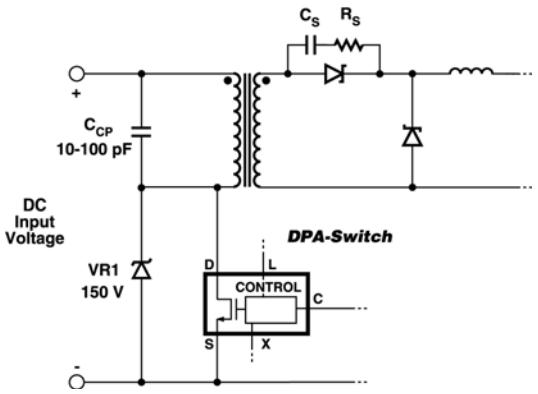


**Figure 9 –** Capacitive clamp and reset circuit

A small capacitor, $C_{CP}$, across the primary winding, clamps the leakage spike during normal operation. Its stored energy is also recycled back into core, as negative flux. In some applications parasitic capacitance alone is sufficient to fulfill this function. Also, in low power applications $C_{CP}$ may not be required. The 150 V Zener, VR1 (a VIN range of 36 to 75 VDC is assumed) only clamps during transients and/or fault conditions.

The value of the reset capacitor $C_S$ can be optimized from the Drain voltage waveforms. If the capacitor is too small (Figure 10) the reset voltage is too high, reaching dangerous levels for the MOSFET and reducing overall efficiency, due to VR1 conducting. If $C_S$ is too large (Figure 11), the reset time may be insufficient, and the switch may start conducting before the flux has been completely reset, ultimately leading to core saturation.

Figure 12 is an optimized Drain voltage waveform. $T_S$ is the entire switching period. It is made up of $t_{ON}$, the MOSFET on-time, $t_{RZ}$ the magnetizing flux reset (to zero) time, $t_{RN}$ the relaxation ring (flux is driven negative) and during $t_{VO}$ the transformer voltage is clamped to zero, by the output diodes. The reset voltage should be kept below 150 V, to avoid VR1 conducting and dissipating power, during normal operation.

The $DC_{MAX}$ reduction function of the *DPA-Switch* is implemented by means of a single resistor connected between the L pin and the input DC rail, as shown in figure 13.

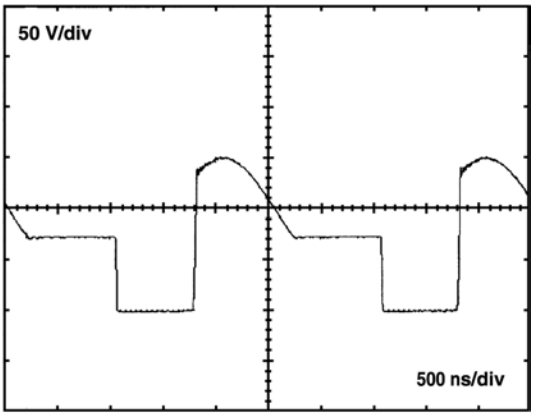


**Figure 10 -** Reset voltage beyond recommended levels. Reset capacitor too small.

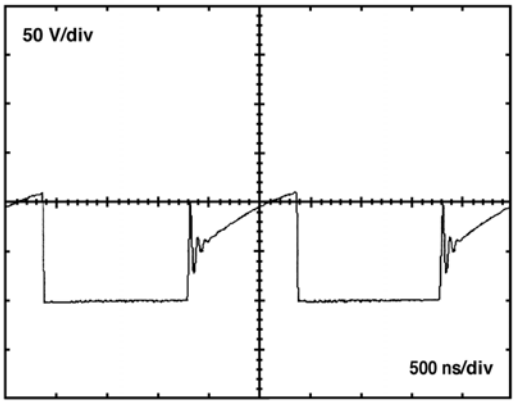


**Figure 11 -** Insufficient reset time. Reset capacitor too large.

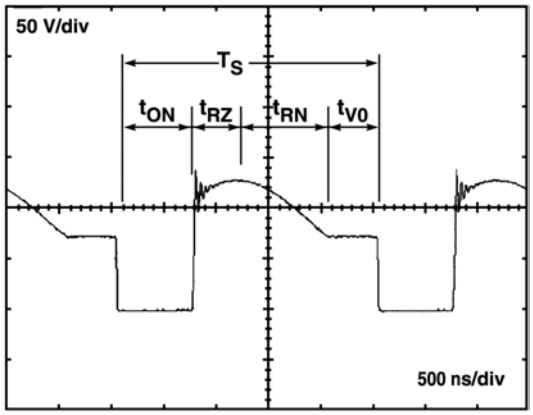


**Figure 12 -** Acceptable Drain voltage waveform.

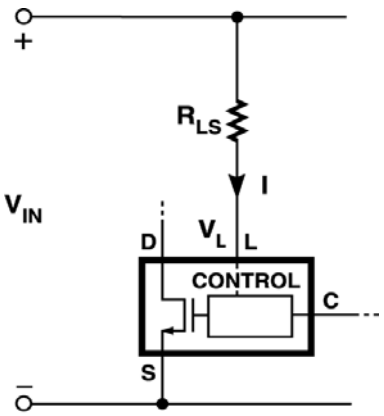


**Figure 13 -** $R_{LS}$ programs $DC_{MAX}$ reduction

As $V_{IN}$ and the current through $R_{LS}$ increases, maximum duty cycle is linearly reduced, as illustrated in figure 14 and by the heavy blue line, in figure 16.

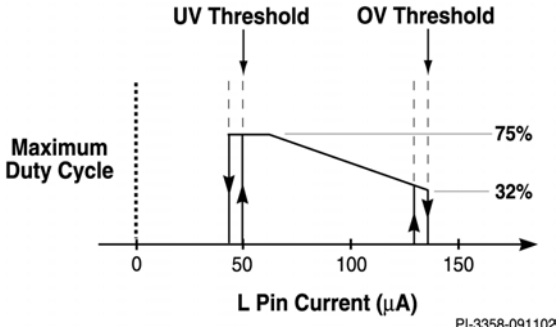


**Figure 14 -** Maximum duty cycle vs. L pin current

At low line, the maximum duty cycle can be as high as 67% (intersection of heavy blue and black curved line), without needing a slope compensation network, because *DPA-Switch* is a voltage mode controlled device. This wide duty cycle at low input voltage minimizes peak and RMS primary currents, increasing efficiency, thermal performance and reliability.

The resistor $R_{LS}$ also sets overvoltage and undervoltage thresholds (see figure 15) with the ratio between the two being internally fixed at 2.7. Extra components can be used to reduce this ratio. The hysteresis on these default thresholds meet ETSI standards.

Figure 16 shows the operating area (double-headed arrow) that the function keeps the maximum duty cycle (the heavy blue line) within. Above the upper boundary, transformer saturation occurs; below the lower curve the controller looses regulation.

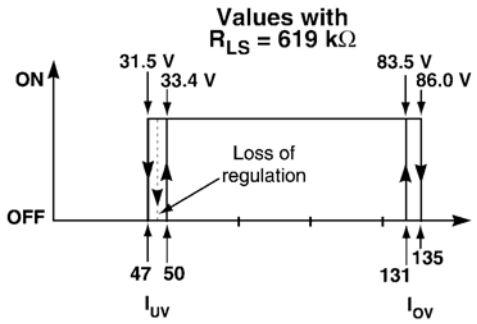


**Figure 15** – UV/OV function vs. L pin current. Both upper & lower UV/OV trip points are shown

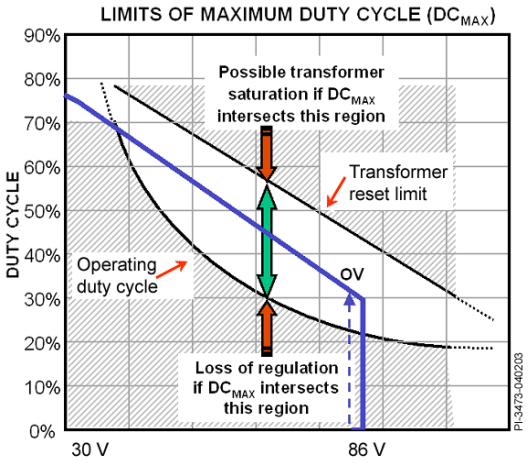


**Figure 16 -** Available range of $DC_{MAX}$ as function of input DC voltage, with an $R_{LS}$ of 619 kΩ

Another advantage of $DC_{MAX}$ reduction is the ability to use a "zero-gap" transformer. This results in lower leakage inductance, less magnetizing energy required and fewer turns, for lower resistive losses in the windings.

At higher output power levels (above 40 W) a resonant reset clamp circuit can be used, maximizing efficiency (see figure 17). This solution recirculates both magnetizing and leakage energy.

As soon as the MOSFET switches off, any energy stored in $C_1$ is passed through the transformer, to the output inductor. When voltage $V_1$ exceeds the DC input voltage, $D_2$ clamps to $V_{IN}$ and $C_1$ is charged by the energy previously stored in the leakage and magnetizing inductance. During the remaining off-time the DRAIN voltage will relax to $V_{IN}$. $C_1$ will retain its peak voltage value of $V_{DS(PK)} – V_{IN}$ unless $V_{DS(PK)} – V_{IN}$ is higher than $V_{IN}$, in which case $D_1$ will clamp the voltage on $C_1$ to $V_{IN}$.

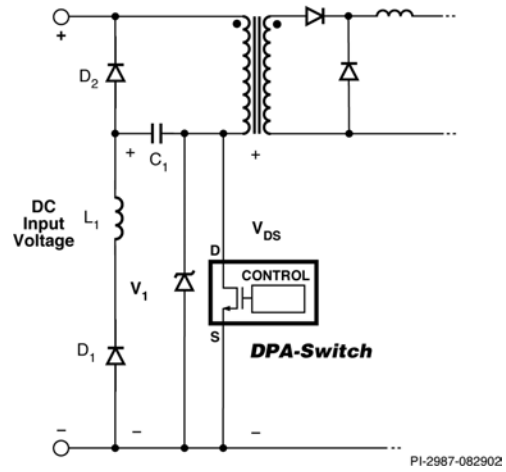


**Figure 17 -** Resonant reset clamp circuit.

When the MOSFET turns on, $V_1$ drops by a delta equal to $V_{IN}$ and goes negative, $C_1$ is recharged via MOSFET, diode $D_1$ and inductor $L_1$ and raises the voltage $V_1$ to an equivalent positive voltage. Once the MOSFET switches off the recycling phase starts all over again.

## Summary

The Capacitor Reset scheme, working in conjunction with the integrated Maximum Duty Cycle reduction feature of the *DPA-Switch*, provides a very simple, robust and highly efficient solution for transformer reset in forward power supply applications. .

## References

[1] DPA 423-426 *DPA-Switch™* family, Product Data Sheet, Power Integrations, Inc., San Jose, CA, September 2002.

[2] *DPA-Switch™* DC-DC Forward Converter Design Guide, Application Note AN-31, Power Integrations, Inc., San Jose, CA, June 2002.